

# MAXIM Engineering Journal

Volume Thirty-Three

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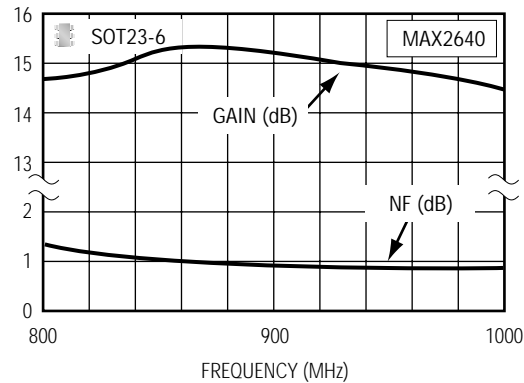
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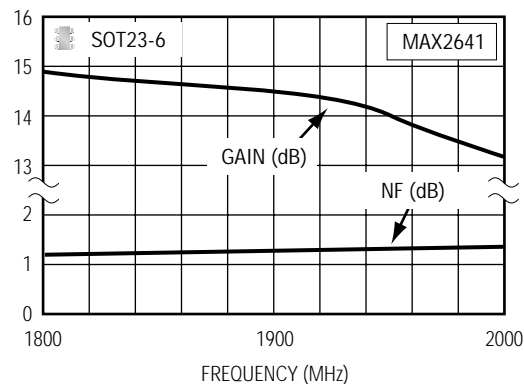
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# Pipeline ADCs come of age

Since the mid-1970s, the majority of monolithic analog-to-digital converters (ADCs) have employed integrating, successive-approximation, and flash techniques. In the 1980s, sigma-delta designs further extended the range of choice. More recently, there has appeared a new class of ADC with an architecture known as “pipeline.” Now offered by several manufacturers, pipeline ADCs offer an attractive combination of speed, resolution, low power consumption, and small die size (which equates to low cost). The features and benefits of this new architecture, are not yet widely understood.

The success of recent ADCs from several manufacturers—including Maxim—indicates that pipeline-architecture (or subranging) ADCs are among the most efficient and powerful data converters available. They offer high speed, high resolution, and excellent performance, along with modest levels of power dissipation and small die size. Within reasonable design limits, they also offer excellent dynamic performance.

This article compares key characteristics of the five most popular techniques for analog-to-digital (A/D) conversion. Also included is an in-depth review of the operation, features, and benefits of pipeline architecture. The article concludes with a design example that features a pipeline ADC in a CCD imaging system.

## Direct-conversion ADCs

Of the five techniques mentioned, one of the fastest is direct conversion, better known as “flash” conversion. ADCs based on this architecture are extremely fast and perform their multibit conversion directly, but they require intensive analog design to manage the large number of comparators and reference voltages required. As shown in **Figure 1**, a converter with N-bit resolution has  $2^N-1$  comparators connected in parallel, with reference voltages set by a resistor network and spaced  $V_{FS}/2^N$  (~1 least significant bit, or LSB) apart.

A change of input voltage usually causes a change of state in more than one comparator output. These output changes are combined in a decoder-logic unit that produces a parallel N-bit output from the converter. Although flash converters are the fastest types available (products like the future MAX104 offer sampling rates to 1GHz), their resolution is constrained by the available

die size and by excessive input capacitance and power consumption caused by the large number of comparators used. Their repetitive structure demands precise matching between the parallel comparator sections, because any mismatch can cause static error such as a magnified input offset voltage (or current).

Flash ADCs are also prone to sporadic and erratic outputs known as “sparkle codes.” Sparkle codes have two major sources:

- Metastability in the  $2^N-1$  comparators
- Thermometer-code bubbles

Mismatched comparator delays can turn a logical 1 into 0 (or vice versa), causing the appearance of “bubbles” in an otherwise normal thermometer code. Because the ADC’s encoder unit cannot detect this error, it generates an out-of-sequence code that also appears as an output “spark.”

Another concern with flash ADCs is die size, which is nearly seven times larger for an 8-bit flash converter than for the equivalent pipelined ADC. In further contrast to pipeline designs, the flash converter’s input capacitance can be six times higher and its power dissipation twice as high.

## Successive-approximation ADCs

The conversion technique based on a successive-approximation register (SAR), also known as bit-weighting conversion, employs a comparator to weigh the applied

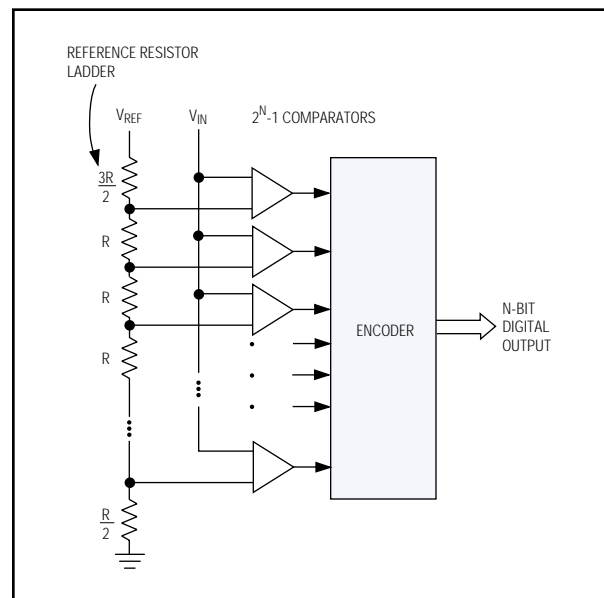


Figure 1. ADCs based on the direct-conversion architecture (better known as flash converters) include  $2^N-1$  comparator banks and a reference resistor-divider network.

input voltage against the output of an N-bit digital-to-analog converter (DAC). Using the DAC output as a reference, this process approaches the final result as a sum of N weighing steps, in which each step is a single-bit conversion.

The first step stores the DAC's most significant bit (MSB) in the SAR, and the next step compares that value (the MSB) against the input. The comparator output (high or low) is fed to the DAC as a correction before the next comparison is made (**Figure 2**). Clocked by a logic control circuit, the SAR continues this weighing and shifting process until it completes the LSB step, which produces a DAC output within  $\pm 1/2\text{LSB}$  of the input voltage. As each bit is determined, it is latched into the SAR as part of the ADC's output.

SAR converters consist of one comparator, one DAC, one SAR, and a logic control unit. They sample at rates to 1MSPS, draw low supply current, and offer the lowest production cost, but their analog design is intensive and time consuming. Compared to a pipelined conversion structure, SAR ADCs provide lower input bandwidth and sampling rates without latency problems.

### Integrating ADCs

Integrating ADCs, also called dual-slope or multislope data converters, are among the most popular converter types. The classic dual-slope converter has two main sections: a circuit that acquires and digitizes the input, producing a time-domain interval or pulse sequence; and a counter that translates the result into a digital output value (**Figure 3**).

The dual-slope converter employs an analog integrator with switched inputs, a comparator, and a counter unit. The input voltage is integrated for a fixed time interval ( $T_{\text{CHARGE}}$ ) that usually corresponds to the maximum count of the internal counter unit (**Figure 4**). At the end of this interval, the device resets its counter and applies an opposite-polarity (negative) reference to the integrator input. With this opposite-polarity signal applied, the integrator "deintegrates" until its output reaches zero, which stops the counter and resets the integrator.

Charge gained by the integrator capacitor during the first, integrating/charging interval ( $T_{\text{CHARGE}}/|V_{\text{IN}}|$ ) must equal that lost during the second, deintegrating/discharging interval ( $T_{\text{DISCHARGE}}/|V_{\text{REF}}|$ ). Then the binary output is proportional to the ratio of these time intervals relative to the full count.  $T_{\text{DISCHARGE}}$  at the end of the second interval corresponds to the ADC's output code. The relationship of  $V_{\text{IN}}$ ,  $V_{\text{REF}}$ ,  $T_{\text{CHARGE}}$ , and  $T_{\text{DISCHARGE}}$  is as follows:

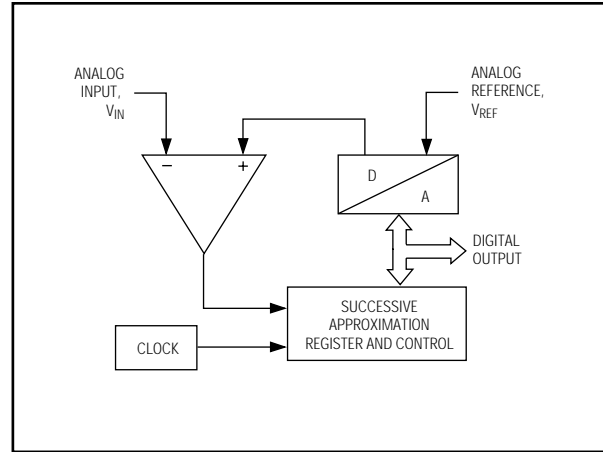


Figure 2. Typical successive-approximation ADCs consist of a single DAC, a comparator, and a successive-approximation register (SAR), plus a clock and logic control.

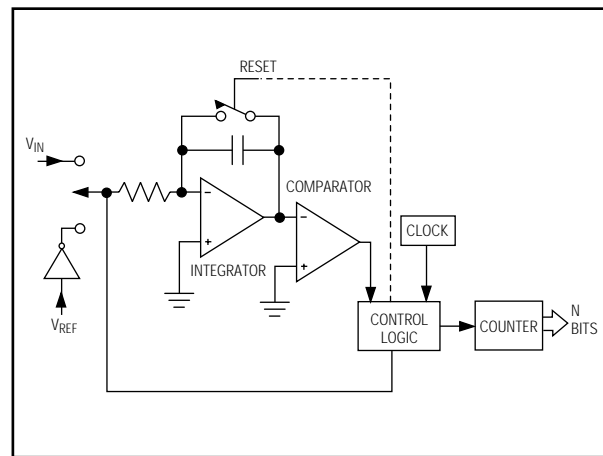


Figure 3. For slowly changing signals, one of the slowest but simplest conversion techniques employs an integrator that charges with the input voltage and discharges with an opposite-polarity reference voltage.

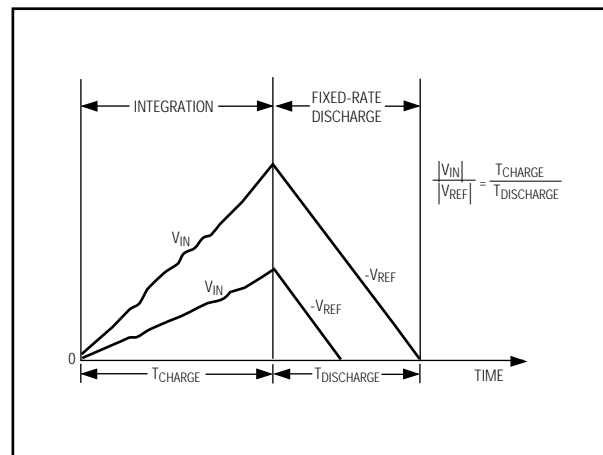


Figure 4. These voltage waveforms illustrate timing relationships for a dual-slope integrating ADC.

$$\frac{|V_{IN}|}{|V_{REF}|} = \frac{T_{CHARGE}}{T_{DISCHARGE}}$$

The system can null any offsets during a conversion by initiating a calibration cycle within the converter. Compared to pipeline ADCs, the integrating types are extremely slow devices with low input bandwidths. But their ability to reject high-frequency noise and fixed low frequencies such as 50Hz or 60Hz makes them useful in noisy industrial environments and applications for which high update rates are not required (e.g., digitizing the outputs of thermocouples).

### Sigma-delta ( $\Sigma$ - $\Delta$ ) ADCs

Sigma-delta ( $\Sigma$ - $\Delta$ ) converters have relatively simple structures. Also called oversampling converters, they consist of a  $\Sigma$ - $\Delta$  modulator followed by a digital decimation filter (**Figure 5**). The modulator, whose architecture is similar to that of a dual-slope ADC, includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. This internal DAC is simply a switch that connects the comparator input to a positive or negative reference voltage. The  $\Sigma$ - $\Delta$  ADC also includes a clock unit that provides proper timing for the modulator and digital filter.

Low-bandwidth signals applied to the input of a  $\Sigma$ - $\Delta$  ADC are quantized with very low (1-bit) resolution, but with a high sampling frequency of 2MHz or higher. Combined with digital post-filtering, this oversampling reduces the sampling rate to about 8kHz and increases the ADC's resolution (i.e., dynamic range) to 16 bits or higher. Although slower than pipeline ADCs and limited to lower input bandwidths, the  $\Sigma$ - $\Delta$  principle has developed a strong position in the data-converter market. It offers three major advantages:

- Low-cost, high-performance conversion
- Integrated digital filter
- DSP-compatible for system integration

### What is a “pipeline” ADC?

Because pipeline ADCs provide an optimum balance of size, speed, resolution, power dissipation, and design effort, they have become increasingly attractive to major data-converter manufacturers and their designers. Also known as subranging quantizers, pipeline ADCs consist of numerous consecutive stages, each containing a

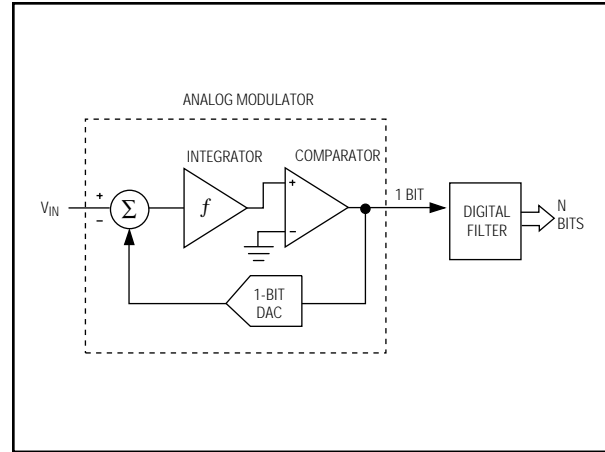


Figure 5. The two major building blocks of a sigma-delta converter are the analog modulator and the digital decimation filter.

track/hold (T/H) amplifier, a low-resolution ADC and DAC, and a summing circuit that includes an interstage amplifier to provide gain.

Target applications for pipeline ADCs include communication systems, in which total harmonic distortion (THD), spurious-free dynamic range (SFDR), and other frequency-domain specifications are relevant; CCD-based imaging systems, in which favorable time-domain specifications for noise, bandwidth, and fast transient response guarantee quick settling; and data-acquisition systems, in which time- and frequency-domain characteristics (i.e., low spurs and high input bandwidth) are both important.

Fast, accurate N-bit conversions can be accomplished using at least two or more steps of subranging (or pipelining). A coarse M-bit A/D conversion is executed first (**Figure 6**). Then, using a DAC with at least N-bit accuracy, the result is converted back to one of  $2^M$  analog levels and compared with the input. Finally, the difference is converted with a “fine” K-bit flash converter and the two (or more) output stages are combined.

The following inequality should be met to correct for overlapping errors:

$$L \cdot M + K > N$$

where L is the number of stages (depending on the manufacturer), M is the coarse resolution of subsequent stages in the ADC/MDAC circuit, K is the fine resolution of the final ADC stage, and N is the pipeline ADC's overall resolution. Most pipeline ADCs include digital error-correction circuitry that operates between the stages.

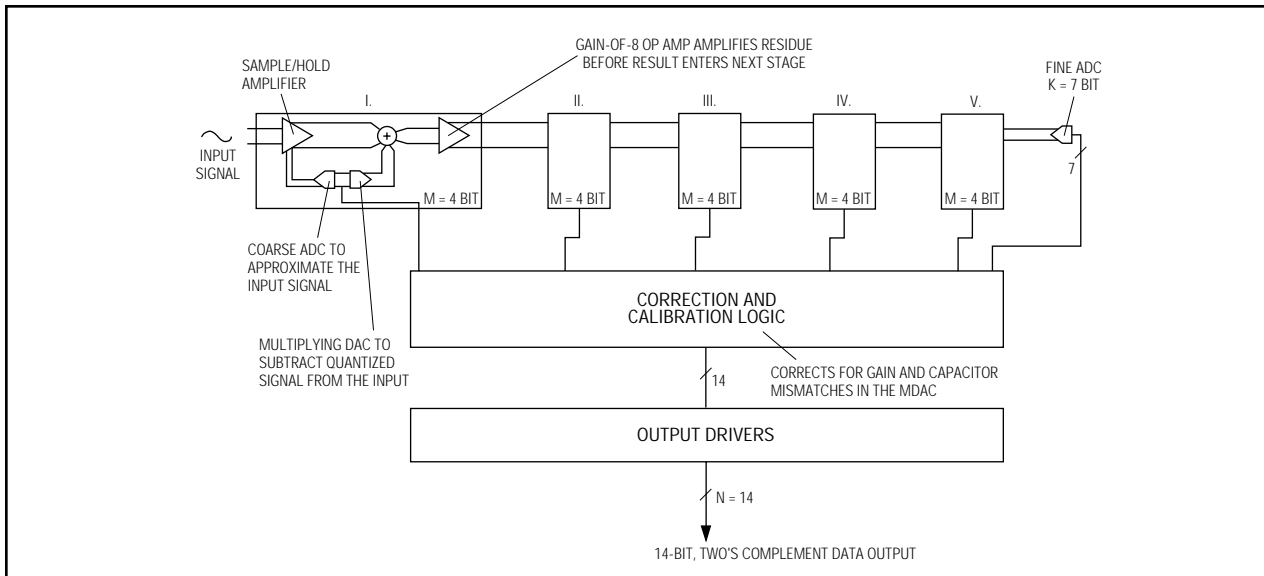


Figure 6. This simplified functional diagram shows the internal error correction and calibration logic for the MAX1200 family of 14-bit, 5-stage pipeline ADCs.

Some pipeline quantizers feature a calibration unit that compensates for unwanted side effects such as temperature drift or capacitor mismatch in the multiplying DAC. This digital calibration is usually performed for several (not all) of the pipeline's consecutive stages, using two adjacent codes that cause a transition equal to  $V_{REF}$  at the MDAC output. Any deviation from this ideal step is an error that can be measured. When all errors have been acquired and accumulated by the subsequent converter stages, they are stored in an on-board memory. Then the results are fetched from RAM during normal operation to redeem gain and capacitor mismatches in the MDAC stages of the pipeline.

As an example, the calibration procedure for Maxim's family of 5-stage pipeline ADCs (MAX1200, MAX1201, and MAX1205) progresses from the pipeline's output to its inputs, just as described in the previous section. Only the first three stages are error-corrected. The third stage is corrected first (to improve linearity), then the second stage is corrected. Those two error-corrected stages then enable calibration of the first stage.

The new pipeline architectures simplify ADC design and provide other advantages as well:

- Extra bits per stage optimize correction for overlapping errors.
- Separate T/H amplifiers for each stage release each previous T/H to process the next incoming sample, enabling conversion of multiple samples simultaneously in different stages of the pipeline.

- Lower power consumption.
- Higher speed ADCs ( $f_{CONV} < 100\text{ns}$ , typical) entail less cost and less design time and effort.
- Fewer comparators to become metastable virtually eliminates sparkle codes and thermometer bubbles.

But pipeline ADCs also impose difficulties:

- Complex reference circuitry and biasing schemes.
- Pipeline latency, caused by the number of stages through which the input signal must pass.
- Critical latch timing, needed for synchronization of all outputs.
- Sensitivity to process imperfections that cause nonlinearities in gain, offset, and other parameters.
- Greater sensitivity to board layout, compared to other architectures.

A multilayer board with properly designed layout can overcome some of these drawbacks. Also important is the selection of external components and the right choice of pipeline ADC—preferably one that includes on-board calibration of both gain and error mismatches (if any) between stages.

## Design Example: Pipeline ADCs in CCD imaging applications

Imaging applications are proliferating, with an annual market growth in excess of 35%. Products include video cameras, camcorders, digital still-cameras, professional video, document scanners, and security systems. These applications employ two primary forms of the imaging sensor:

- CMOS imaging elements
- Charge-coupled devices (CCDs)

CMOS-based elements remove some of the constraints associated with CCDs, such as noise and temperature-coefficient considerations. Their pixels can be read one by one, but this reading frequency is limited to 30 frames per second and the output requires special design-intensive pixel processing.

CCDs are used in most of today's applications because they provide the best sensitivity and dynamic range. CCD resolution ranges from 1x256 to 512x512 pixels and even higher. To capture the incoming photons, each pixel consists of one "charge bucket" (three in an RGB CCD).

The CCD is the central element in an imaging system. All other circuitry simply supports the stringent and specific signal conditioning necessary to achieve maximum performance. Typical output signal levels for a CCD are very low, and they suffer from the detrimental effects of various noise sources. Designers must be aware of these characteristics and the special techniques needed to manage them effectively.

In a typical CCD system (**Figure 7**), the CCD output is a serial stream of pixel "charges," shifted at high rates from the typical CCD format to one of stepped DC-voltage levels. This sequence of pulses rides on a DC

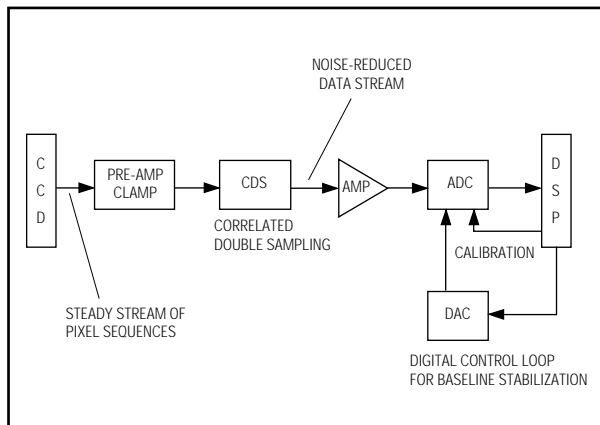


Figure 7. This simplified block diagram shows the major components of a typical CCD system.

bias (or offset voltage) of 10V or higher. For this reason, CCD outputs are capacitively coupled to the lower voltage downstream signal-processing elements. Prior to preamplification and processing, a clamp or DC-restoration circuit is necessary to maintain the "dark baseline" level that corresponds to zero pixel charge.

Noise, the main restriction on sensitivity and dynamic range in a CCD application, must be carefully controlled. Noise sources include:

- $kT/C$  noise, caused by FET switching resistance ( $R_{ON}$ ) in the CCD output
- Circuit noise,  $1/f$  noise, and shot noise
- Quantization noise ( $q/\sqrt{12}$ )
- 60Hz AC-line interference
- White or thermal noise caused by resistors and conductors in the circuitry:  $e_{WN} = \sqrt{4kTBR_{OUT}}$ , where

$$k = 1.38054 \cdot 10^{-23} \text{ (Boltzmann's constant)}$$

$$T = \text{temperature in degrees Kelvin} \\ (298^\circ\text{K} = +25^\circ\text{C})$$

$$B = \text{noise bandwidth (Hz)}$$

$$R_{OUT} = \text{CCD output-stage resistance} \\ (R_{OUT} = R_L + R_{ON})$$

where  $R_L$  is the load resistor and  $R_{ON}$  represents the FET's on-resistance.

### Processing the CCD output

The CCD output is not a continuous periodic waveform, but resembles a series of steps with different amplitudes or DC levels (**Figure 8**). In each cycle, pixel information is contained in the lower portion of the waveform. For circuit elements in the signal processing chain, including

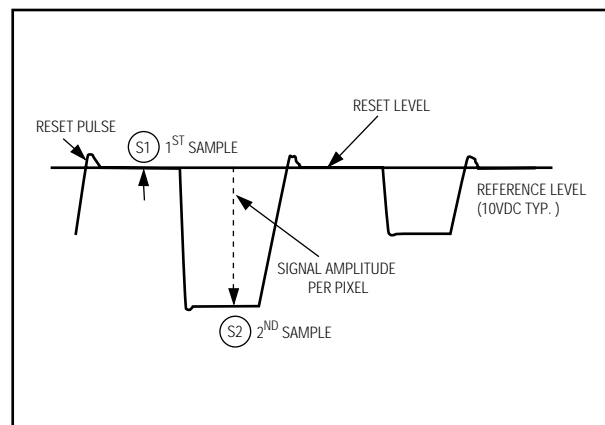


Figure 8. Each cycle of the CCD output signal contains pixel information in the lower portion of the waveform.

the ADC, the characteristics of this waveform dictate that time-domain rather than frequency-domain specifications are the primary concern. Following the CCD element, a preamplifier boosts the signal level and a clamp restores the DC reference (black) level.

As mentioned earlier, the dominant kT/C noise is most significant in limiting the effective resolution in a CCD imaging system. To reduce this noise, the signal path should include a unit for correlated double-sampling (CDS). This name is taken from the double-sampling approach used to remove unwanted noise components: a sample (S1) is taken at the end of the reset period shown in Figure 4, and a second sample (S2) is taken during the information portion of the signal. The two samples differ only by a voltage representing the charge signal minus the noise. (Further discussion of the CDS unit is beyond the scope of this article.)

Following the CDS element can be a buffer/driver stage, which provides the correct full-scale and common-mode input to the quantizer (ADC) stage. The ADC is a performance-critical component in the signal processing chain. It must supply high resolution with excellent

linearity, low noise, low drift, and low offset. All this performance is necessary to ensure image quality, color purity, and freedom from distortion over time.

Scientific and medical imaging generally requires even higher resolution and dynamic range. To establish accurate and detailed images of scanned objects, these applications employ larger arrays with more pixels and longer frame-update times. They require ADCs with good linearity, low offset, and lower speed but higher resolution—such as the MAX1201/MAX1205 from Maxim. These 14-bit, 2.2MSPS/1.1MSPS monolithic ADCs meet the necessary linearity and accuracy specifications. Their very low DNL error ( $\pm 0.3\text{LSB}$ ) and self-calibration on demand provide a cost-effective alternative to expensive hybrids in demanding, high-resolution imaging applications. **Table 1** describes Maxim's latest generation pipeline ADCs.

In summary, **Table 2** recaps the major ADC types available today. To order Maxim product samples for your evaluation, use the Business Reply Card in this issue.

**Table 1. Typical performance for Maxim's latest generation of pipeline ADCs**

PARAMETER	MAX1201	MAX1205	MAX1200
Architecture	DIFFERENTIAL PIPELINE	DIFFERENTIAL PIPELINE	DIFFERENTIAL PIPELINE
Number of stages	5	5	5
Resolution	14 Bits	14 Bits	16 Bits
Sampling rate	2.2MSPS	1MSPS	1MSPS
Power dissipation	269mW	257mW	273mW
Input FS range (diff.)	$\pm V_{REF}$	$\pm V_{REF}$	$\pm V_{REF}$
Small-signal input BW	78MHz	78MHz	78MHz
Full-power input BW	3MHz	3MHz	3MHz
INL	$\pm 1.2\text{LSB}$	$\pm 1.2\text{LSB}$	$\pm 0.5\text{LSB}$
DNL	$\pm 0.3\text{LSB}$	$\pm 0.3\text{LSB}$	$\pm 0.7\text{LSB}$
SNR@ $f_{IN} = 500\text{kHz}$	82dB	80dB	83dB
SFDR@ $f_{IN} = 500\text{kHz}$	85dB	87dB	88dB
THD@ $f_{IN} = 500\text{kHz}$	-82dB	-84dB	-85dB
SINAD@ $f_{IN} = 500\text{kHz}$	78dB	78dB	81dB
On-chip calibration	✓	✓	✓
Three-state output	✓	✓	✓
Package type	44MQFP	44MQFP	44MQFP



**Table 2. Major analog-to-digital conversion techniques**

SYSTEM ARCHITECTURE	RESOLUTION	SPEED	MAXIM ADCs	ADVANTAGES/DRAWBACKS
Flash	8 bits	250Msps–1Gsps	MAX100 MAX101A MAX104*	+ Extremely fast + High input bandwidth - Highest power consumption - Large die size - High input capacitance - Expensive - Sparkle codes**
SAR	10 bits–16 bits	76ksps–250ksps	MAX195 MAX144/MAX145 MAX115* MAX157/MAX159 MAX186/MAX188	+ High resolution and accuracy + Low power consumption + Few external components - Low input bandwidth - Limited sampling rate - $V_{IN}$ must remain constant during conversion
Integrating	> 18 bits	< 50ksps	MAX132 MAX135	+ High resolution + Low supply current + Excellent noise rejection - Low speed
Sigma-Delta ( $\Sigma$ - $\Delta$ )	> 16 bits	> 200ksps	MAX1400 MAX1401* MAX1402* MAX1403*	+ High resolution + High input bandwidth + Digital on-chip filtering - External T/H - Limited sampling rate
Pipeline	12 bits–16 bits	1Msps–80Msps	MAX1200 MAX1201 MAX1205	+ High throughput rate + Low power consumption + Digital error correction and on-chip self-calibration - Requires 50% duty cycle typical - Requires minimum clock frequency

\*Future product—contact factory for availability.

\*\*Sparkle codes are erratic errors caused by metastable comparators or out-of-sequence output codes (thermometer bubbles), which in turn are

# DESIGN SHOWCASE

## Low-cost step-up/step-down converter accepts 2V to 16V inputs

The circuit shown in **Figure 1** is a low-cost step-up/step-down DC-DC converter. By definition, its input voltage can range above and below the regulated output voltage. The circuit includes a simple switch-mode boost converter (IC1) that contains a comparator, normally used to detect low battery voltage. In this example, the comparator controls an external, low-cost pnp transistor operating as a linear regulator.

IC1 steps up  $V_{IN}$  (2V min) to the level of  $V_X$  as determined by the jumper block JU1. A 2-3 jumper selects the internal divider, producing  $V_X = 12V$ , and a 2-1 jumper selects feedback resistors R1 and R2, producing  $V_X = 1.5V(R1 + R2)/R2$ .  $V_X$  should be set 1V to 2V above the desired output voltage.

Linear regulator Q1 steps down  $V_X$  to an output level set by R3 and R4:

$$V_{OUT} = 1.5V(R3 + R4)/R4$$

where  $V_X > V_{OUT}$ .

When  $V_{IN} > V_X$ , the switching regulator stops and the linear regulator alone controls  $V_{OUT}$ . C6 reduces output ripple. This circuit allows a wide range of input and output voltages, and delivers output currents up to 500mA (**Figure 2**).

*A similar idea appeared in the 7/16/98 issue of Electronic Design.*

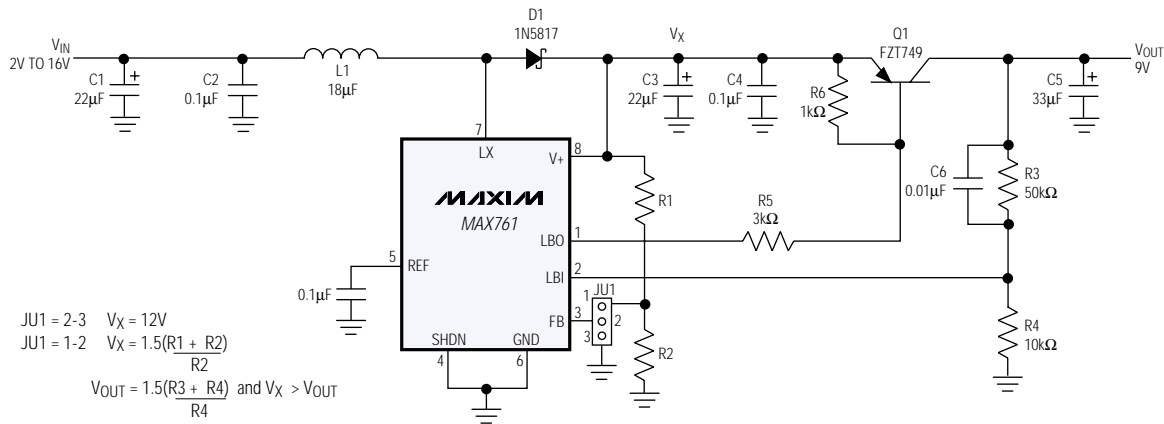


Figure 1. This step-up/step-down converter maintains a regulated output (set to 9V for the R3/R4 values shown) as the input voltage varies between 2V and 16V.

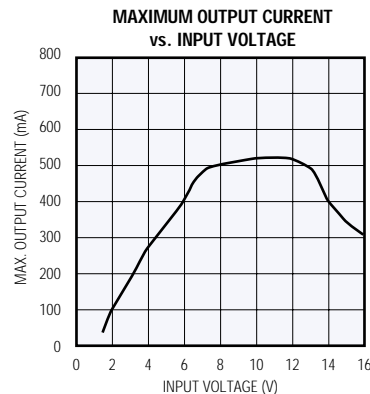


Figure 2. For  $V_{OUT} = 9V$ , the maximum output current in Figure 1 varies with input voltage, as shown.

## DESIGN SHOWCASE

# Visible-laser driver has digitally controlled power and modulation

Many laser diodes include a photodiode that generates a current proportional to the intensity (optical power) of the laser beam. Most of these photodiodes, however, have relatively slow response times and cannot track the peak optical power of a typical modulated laser diode. Instead, the driver circuits for these devices control the laser by monitoring a relative average optical power.

The circuit shown in **Figure 1** includes a 10-bit digital-to-analog converter (DAC) with 3-wire serial input that operates and maintains a visible-light laser diode at constant average optical output power. A separate digital input line (MOD) enables a

comparator with open-drain output (IC4) to implement digital communications by pulsing the laser-diode through Q1. Circuit components were chosen to minimize the layout area and cost.

Resistor R6 converts the photodiode current to a usable voltage, which is applied to the inverting input of a “leaky” integrator based on the high-speed op amp IC3. The integrator smoothes out variations in the modulation and prevents the feedback loop from trying to regulate the laser pulses. The integrator is made leaky (by R10) to ensure compensation of downward as well as upward variations in the average power.

[continued]

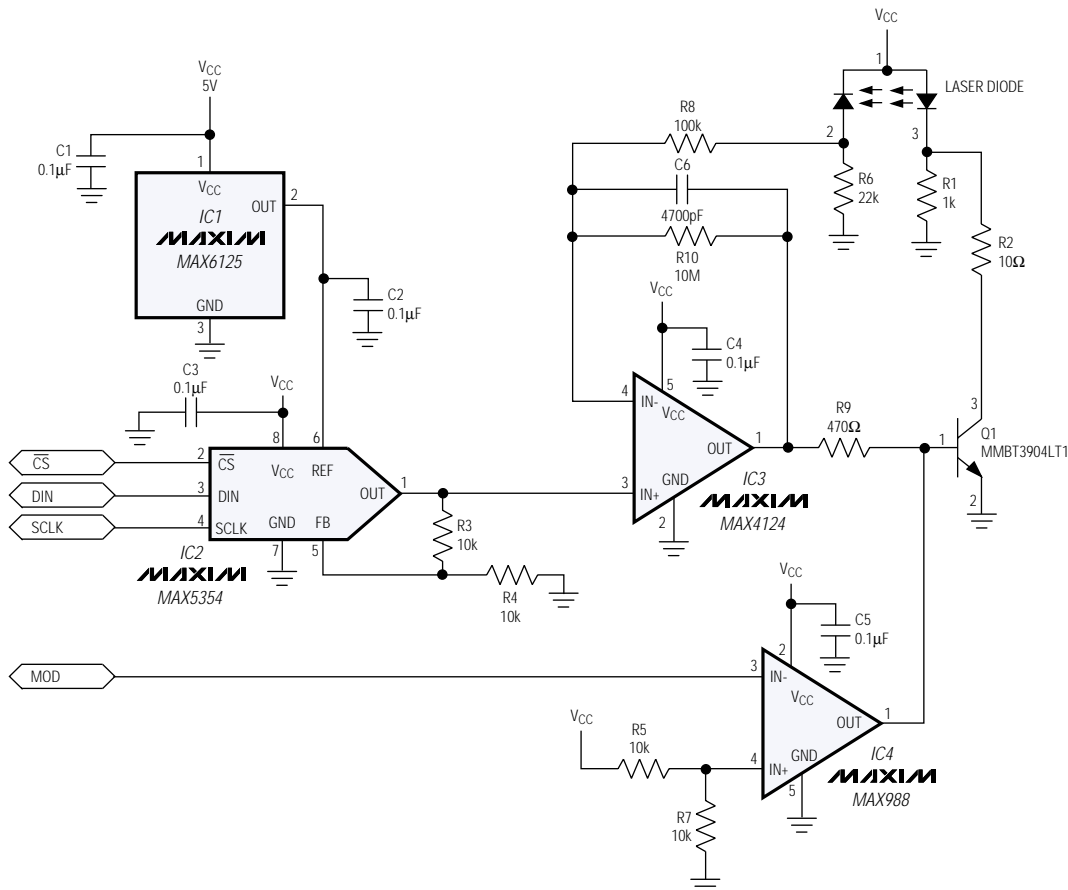


Figure 1. This circuit provides digital control of the modulation and power output of a visible-light laser diode.

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Thus, the integrator creates an error signal and base drive for Q1 by monitoring the voltage across R6 and comparing it to the DAC's preset voltage. The DAC's reference voltage (from IC1) is 2.5V, but its output-voltage buffer has a gain of 2V/V, giving the DAC output an adjustment range of 0 to 5V. With its nominal base voltage set by the DAC output, Q1 controls the optical power by regulating current through the laser diode.

R9 provides isolation and helps to stabilize IC3 when the base of Q1 is being shorted and released by a signal from the MOD input. By maintaining a small

laser-diode current during the "off" periods of digital modulation, R1 preempts another problem: startup time for a laser diode increases tremendously if the forward current goes to zero. R1 ensures that the laser current is below the threshold for lasing, but high enough to allow an acceptable turn-on time for communication and modulation.

*A similar idea appeared in the 3/23/98 issue of Electronic Design.*

# DESIGN SHOWCASE

## High-voltage circuit breaker protects to 26V

Widespread use of the Universal Serial Bus (USB) has led to a selection of overcurrent-protection circuits for supply rails in the +2.7V to +5.5V range, but few products are available for voltages above that range. The circuit breaker in **Figure 1** operates on supply voltages to +26V and trips at a programmed current threshold.

IC1 is a high-side current-sense amplifier that monitors supply current via the voltage across R2 and generates a proportional but smaller current at the OUT terminal:

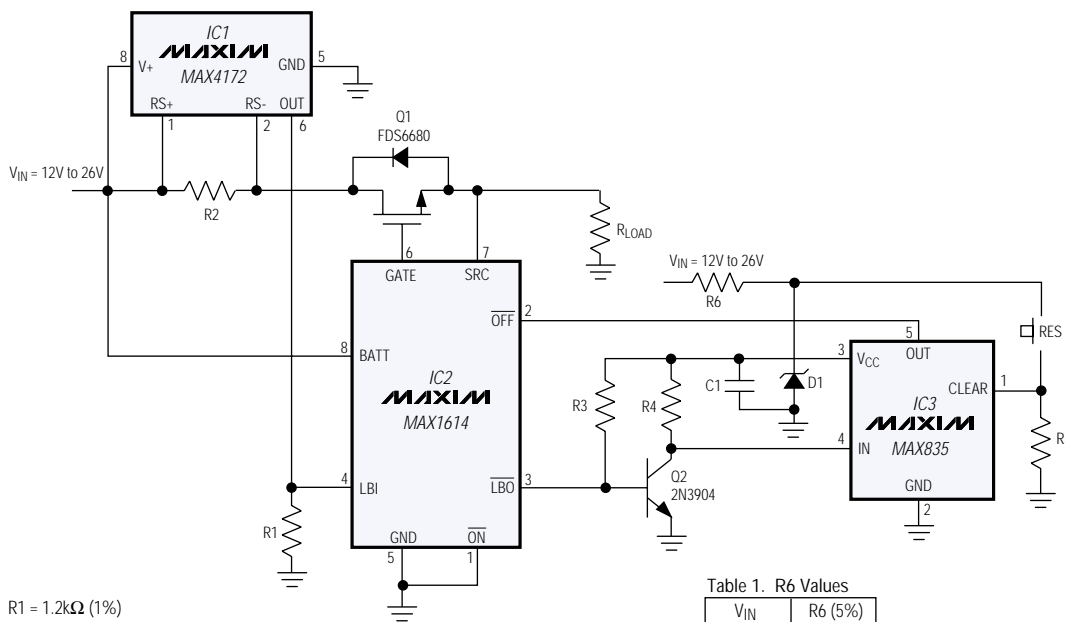
$$I_{OUT} = (R2 \cdot I_{TRIP})/100.$$

R1 and R2 determine the trip current:

$$R1 = 120/(R2 \cdot I_{TRIP}).$$

R1 in the figure was chosen for a trip current of 1A, but values to 10A are acceptable. Supply current at the trip level produces a voltage across R1 that triggers the “low-battery” comparator in IC2 (a high-side, N-channel MOSFET driver). The comparator output (LBO) turns on Q2 to saturation, causing the latched output of IC3 (a micropower voltage monitor) to go low. Applied to IC2’s pin 2, this signal disconnects the power by turning off Q1.

[continued]



- R1 = 1.2kΩ (1%)
- R2 = 100mΩ
- R3 = 68kΩ (5%)
- R4 = 6.8kΩ (5%)
- R5 = 100kΩ (5%)
- R6 = SEE TABLE 1
- Q1 = FDS6680
- Q2 = 2N3904
- D1 = 1N5997B (7.5V)
- C1 = 0.01µF

Table 1. R6 Values

V <sub>IN</sub>	R6 (5%)
26V	3kΩ
24V	2.7kΩ
20V	2kΩ
15V	1.2kΩ
12V	750Ω

Figure 1. This circuit provides overcurrent protection for supply-rail voltages to +26V.

Power remains off until IC3 is unlatched (by depressing the reset button). (You may also need to push the button following initial power-up, to ensure the correct circuit state at that time.) Choose R6 according to **Table 1** (in Figure 1) for supply voltages of +12V and above. For supply voltages below

+12V, D1 and R6 are not required. The signal delay from IC3 to the load (via IC2 and Q1) is as follows: turn-off time is about 5 $\mu$ s (**Figure 2a**), and turn-on time is about 400 $\mu$ s (**Figure 2b**).

*A similar idea appeared in the 9/11/98 issue of EDN.*

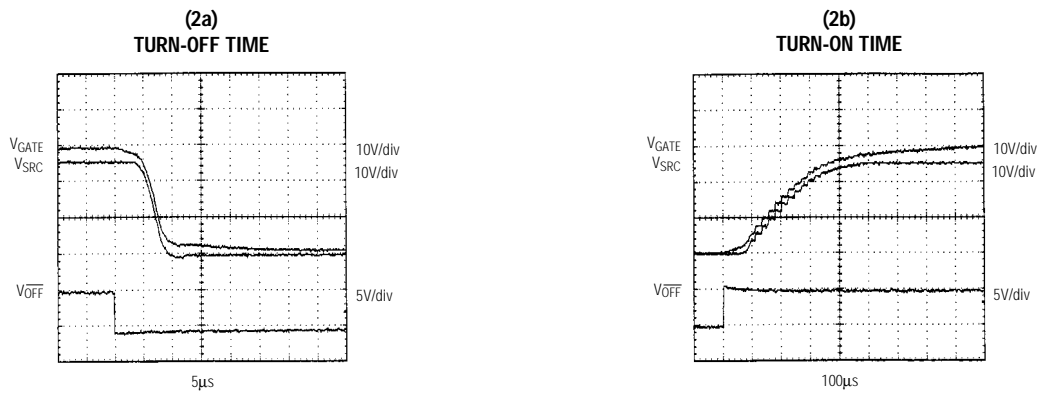


Figure 2. With Figure 1's load-current trip threshold set at 1A, the load voltage (middle waveform) turns off (a) and on (b), as shown. ( $V_{OFF}$  is the signal at IC2, pin 2.)

# DESIGN SHOWCASE

## Dual comparator forms temperature-compensated proximity detector

In the proximity detector shown in **Figure 1**, a 4-inch-square piece of copper-plated PC board serves as an antenna that forms one plate of a capacitor. An approaching (grounded) person serves as the other plate, producing a capacitance value (in the 2pF to 5pF range) that increases as the person approaches. At 6 inches from the copper plate, for example, the person produces a capacitance value of about 2pF.

The method for transforming this proximity distance into a proportional voltage is illustrated by a simplified circuit that lacks temperature compensation (**Figure 2**). Transitions of the input square wave apply directly to the lower input of the exclusive-OR (XOR) gate, but are delayed  $0.693(R1)(C1)$  seconds before being reconstructed by the comparator and applied to the upper input. R4 and C2 filter the resulting XOR output to produce a voltage proportional to distance.

[continued]

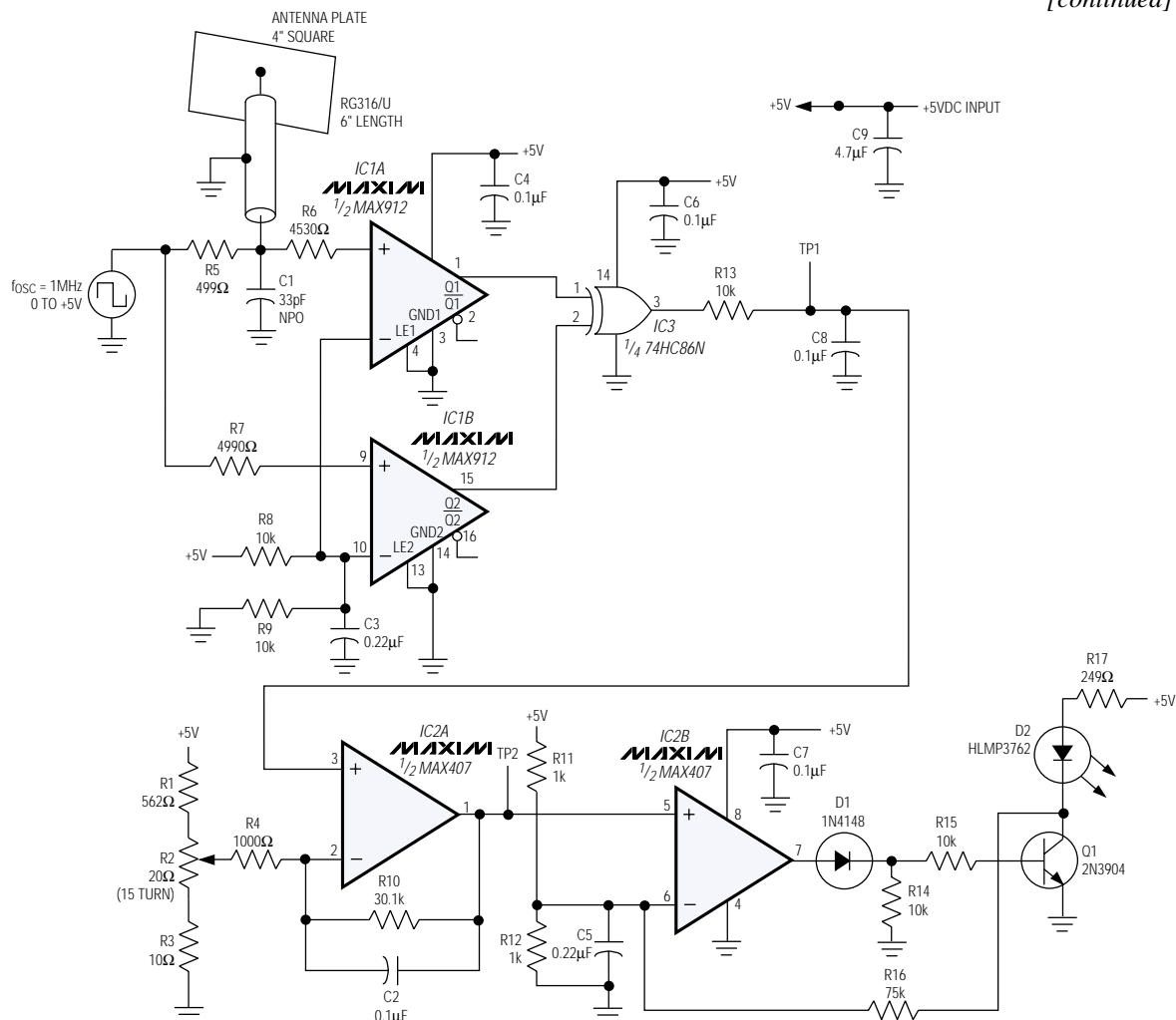


Figure 1. This proximity detector lights the LED when a person approaches the antenna plate within a threshold set by the potentiometer.

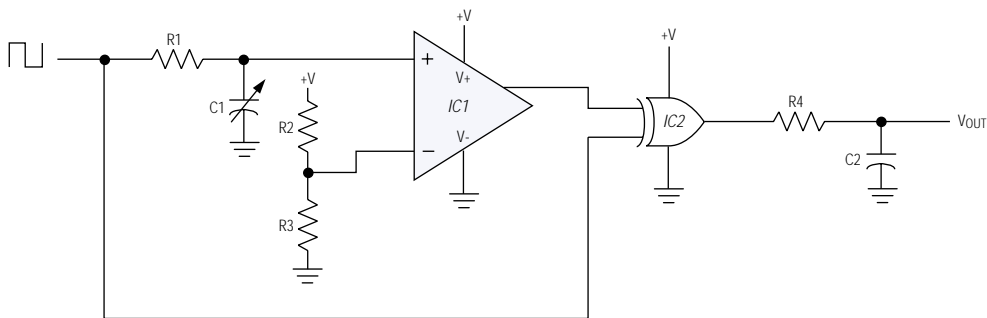


Figure 2. This circuit, uncompensated for temperature, illustrates the principle of capacitance-to-voltage conversion.

The XOR output's duty cycle is proportional to the sum of  $R1 + C1$  delay plus comparator propagation delay, so a small variation in comparator delay can mask small changes in antenna capacitance. The Figure 1 circuit overcomes this limitation with a dual comparator (IC1). Passing the XOR inputs through nearly identical comparators largely nullifies the effect of offset voltage, drift, and propagation delay through the comparators.

Figure 1's delay capacitance consists of a 33pF capacitor (C1) in parallel with 15pF (6 inches of coaxial cable at 30pF per foot) and the 4-inch-square antenna plate. It charges to 5V via R5 during each positive half cycle of the input square wave. When no body is near the detector, this capacitance equals 48pF and produces a delay of 16.5ns at the upper XOR input. With a hand placed 6 inches from the detector, the capacitance rises to 50pF and produces a delay of 17.3ns, yielding a time difference of only 0.8ns.

To detect such small time differences—over temperature and with accuracy—the comparators must be

very stable in offset voltage and propagation delay (delay time is affected by changes in offset voltage as well as propagation delay). A single 10ns comparator is generally stable to within 1ns, but resolving subnanosecond intervals requires the dual-comparator approach of Figure 1, which increases the useful resolution by a factor of four to five.

Op amp IC2A offsets and amplifies the DC voltage at TP1, which corresponds to the distance between a hand and the antenna plate. A hand movement toward the antenna causes the voltages at TP1 and TP2 to rise. Op amp IC2B and the transistor serve as a comparator with hysteresis, which compares the TP2 voltage with 2.5V. Thus, any TP2 voltage above 2.5V (which corresponds to a proximity of 6 inches) turns on the LED. The potentiometer (R2) can be adjusted to set a threshold other than 6 inches, and a DVM at TP2 can be connected to read out the proximity in inches (for example). R16 adds hysteresis to ensure a well-defined transition.

[continued]

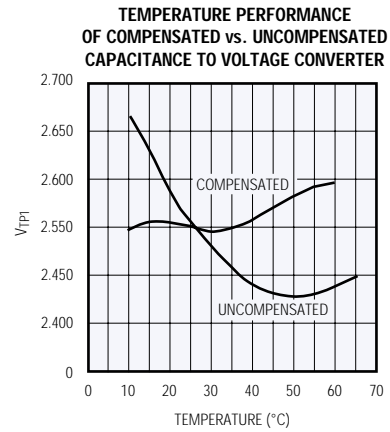


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To compare the compensated and uncompensated circuits for temperature stability, adjust the Figure 1 potentiometer to 2.5V, then measure TP2 of Figure 1 (compensated) and TP1 of Figure 2 (uncompensated) at various temperatures (**Figure 3**). To ensure frequency stability for the high-speed dual comparator in Figure 1, the copper-clad PC board should have a ground layer in addition to the circuit layer. Power-supply bypassing should include 0.1 $\mu$ F ceramic capacitors placed very close to the comparators' supply terminals.

*A similar idea appeared in the 2/16/98 issue of EDN.*



*Figure 3. The dual-comparator technique of Figure 1 offers much better temperature stability than that of the uncompensated circuit in Figure 2.*

# NEW PRODUCTS

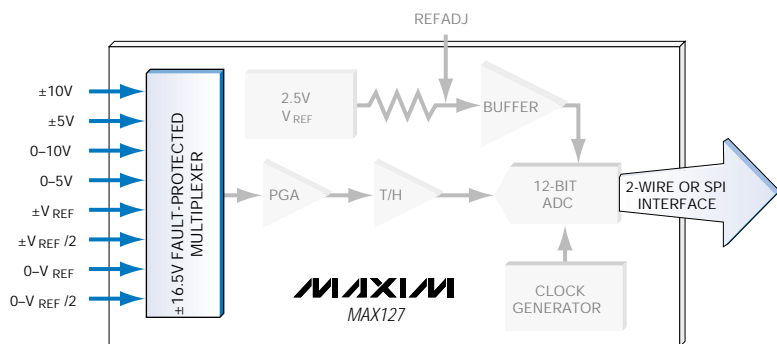
## Multirange, +5V, 12-bit DASs have 2-wire serial interface

The MAX127/MAX128 12-bit data-acquisition systems (DASs) operate on a single +5V supply and accept analog inputs that range above the power-supply rail and below ground. Each device has eight analog input channels that are independently software-programmable for a variety of ranges:  $\pm 10V$ ,  $\pm 5V$ , 0 to 10V, or 0 to 5V for the MAX127; and  $\pm V_{REF}$ ,  $\pm V_{REF}/2$ , 0 to  $V_{REF}$ , or 0 to  $V_{REF}/2$  for the MAX128.

The range-switching feature increases the effective dynamic range to 14 bits and provides the flexibility to interface a 5V system with sensors powered by  $\pm 12V$ ,

$\pm 15V$ , or a 4–20mA current loop. Fault protection to  $\pm 16.5V$  protects the conversion results on a selected channel from a fault on any other channel. Other features include a track/hold with 5MHz bandwidth, an 8ksps throughput rate, and a choice of external reference or the internal 4.096V reference.

A 2-wire serial interface allows communication among multiple devices. A hardware shutdown input (SHDN) and two software-programmable power-down modes (standby and full power-down) enable low-current shutdowns between conversions. To eliminate start-up delays, the reference buffer remains active during standby mode. The MAX127/MAX128 devices are available in 24-pin DIPs or space-saving 28-pin SSOPs. Prices start at \$9.25 (1000 up, FOB USA).



## 1Msps, 14-bit, self-calibrating ADC operates on +5V

The MAX1205 is a 14-bit monolithic-CMOS ADC that operates on +5V and is capable of conversion rates to 1Mbps. Its fully differential pipelined architecture includes digital error correction and a short self-calibration procedure, which together ensure 14-bit linearity at full sample rates. At 100kHz, the device exhibits an 83dB SNR and 91dB SFDR. A built-in track/hold input stage maintains superb dynamic performance up to the Nyquist frequency.

The MAX1205 differential inputs accept signal swings to  $\pm V_{REF}$ . A single-ended input is possible, but the differential configuration is recommended for optimum

performance. (Note that two op amps can be used to generate a fully differential signal from a single-ended source.) The reference input is also differential, with sense pins (RFPS, RFNS) that enable the device to compensate for any resistive-divider action due to finite resistance in the chip and the external traces.

Operating with a +5V  $\pm 5\%$  supply and a sampling rate of 1Msps, the MAX1205 typically dissipates 260mW. Its 14-bit, two's complement, three-state output data is CMOS-compatible. For higher speed (to 2.2Msps), choose the pin-compatible upgrade MAX1201. The MAX1205 is available in a 44-pin MQFP package, with prices starting at \$11.50 (1000 up, FOB USA).

## +5V, 2.2Msps, 14-bit ADC provides self-calibration and digital error correction

The MAX1201 is a 14-bit monolithic CMOS analog-to-digital converter (ADC) that operates on 5V and is capable of conversion rates to 2.2Msps. Its 14-bit linearity at full sample rates is ensured by a fully differential pipelined architecture with digital error correction and on-demand self-calibration. An internal track/hold maintains superb dynamic performance up to the Nyquist frequency.

The MAX1201's fully differential inputs allow maximum swings of  $\pm V_{REF}$  centered on a selectable common-mode voltage. The device can operate with single-ended inputs as well, though with somewhat reduced dynamic performance. The addition of two external op amps converts a single-ended source to the fully differential source recommended for optimum performance. The reference input is also differential. Sense pins RFPS and RFNS enable compensation for resistive-divider action due to reference-pin source resistance, or finite resistance in the external reference traces, or both.

The MAX1201's dynamic performance includes a signal-to-noise ratio of 83dB, a spurious-free dynamic range of 91dB, a differential nonlinearity error of  $\pm 0.3LSB$ , and an integral nonlinearity error of  $\pm 1.2LSB$ . Typical power consumption with a 5V  $\pm 10\%$  supply and 2.2Msps sampling rate is only 295mW. The 14-bit-parallel, two's complement output data is CMOS-compatible and three-statable. The MAX1201 is available in a 44-pin MQFP package, with prices starting at \$39.96 (1000 up, FOB USA).

# NEW PRODUCTS

## Multirange, 8-channel, 12-bit DASs operate on +5V

The 12-bit MAX1270/MAX1271 DASs operate on a single +5V supply, yet their analog input ranges extend above the power-supply rail and below ground. For each device, the eight analog channel inputs are independently software-programmable. The MAX1270 offers  $\pm 10V$ ,  $\pm 5V$ , 0 to 10V, and 0 to 5V, and the MAX1271 offers  $\pm V_{REF}$ ,  $\pm V_{REF}/2$ , 0 to  $V_{REF}$ , and 0 to  $V_{REF}/2$ . The maximum throughput rate is 110ksps.

The MAX1270/MAX1271 range-switching capability not only increases the dynamic range to 14 bits, it also provides the flexibility to interface a 5V system with sensors powered by  $\pm 12V$ ,  $\pm 15V$ , or a 4–20mA current loop. The converters also include fault protection to  $\pm 16.5V$ , which ensures that the selected channel remains unaffected by a fault condition on any other channel. Other features include a track/hold with 5MHz bandwidth, a software-selectable internal/external clock, and the option to operate with an external reference instead of the internal 4.096V reference.

The MAX1270/MAX1271 have a 4-wire serial interface that connects directly to SPI™/QSPI™ and MICROWIRE™ devices without external logic. To implement a low-current shutdown between conversions, both converters provide a hardware-shutdown input (SHDN) as well as two software-programmable power-down modes: standby (STBYPD), and full power-down (FULLPD). To eliminate start-up delays, the reference buffer remains active during the standby mode.

The MAX1270/MAX1271 devices are available in 24-pin DIP or 28-pin SSOP packages. Prices start at \$8.95 (1000 up, FOB USA).

*SPI and QSPI are trademarks of Motorola, Inc.*

*MICROWIRE is a trademark of National Semiconductor Corp.*

## Low-cost SOT23-3 voltage references have low dropout and low power

The MAX6001/MAX6002/MAX6004/MAX6005 low-cost voltage references are available in tiny 3-terminal SOT23 packages. Each series-mode device combines the power savings of series operation with the cost of a shunt-mode device. But unlike conventional 2-terminal, shunt-mode references that are biased at the load current and require an external resistor, the MAX6001 family of references eliminates the resistor and generates a current that is virtually independent of the supply voltage. For further space savings, internal compensation eliminates the need for an external compensation capacitor.

## SOT23-3 voltage references offer tight accuracy and low tempco

The MAX6012/MAX6021/MAX6025/MAX6041/MAX6045/MAX6050 series of precision, low-dropout, micropower voltage references are available in tiny SOT23-3 packages. They offer voltage options of 1.250V, 2.048V, 2.500V, 4.096V, 4.500V, and 5.000V. Their proprietary curvature-correction circuit and laser-trimmed thin-film resistors provide a low temperature coefficient ( $<20\text{ppm}/^\circ\text{C}$ ) and tight initial accuracy.

Unlike conventional shunt-mode (2-terminal) references that waste supply current and require an external resistor, these series-mode devices require no external resistor. Drawing only  $27\mu\text{A}$  of quiescent supply current, they can sink or source load currents as high as  $500\mu\text{A}$ .

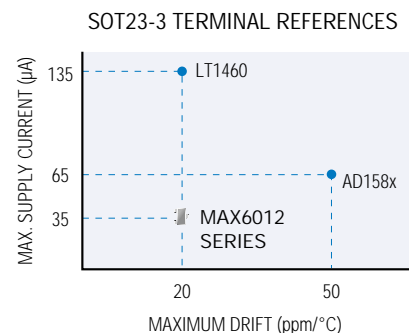
Because they require no external compensation capacitor, members of the internally compensated MAX6012 family of references save valuable board area in

These references are intended for high-volume, cost-sensitive, 3V and 5V battery-operated systems that exhibit wide variations in supply voltage and require very low power dissipation. Applications include notebook computers, cellular phones, pagers, hard-disk drives, PDAs, GPSs, and DMMs. The references accept input voltages up to 12.6V, and produce outputs of 1.250V (MAX6001), 2.500V (MAX6002), 4.096V (MAX6004), and 5.000V (MAX6005).

Performance includes a maximum initial accuracy of 1%, a maximum temperature coefficient of  $100\text{ppm}/^\circ\text{C}$ , a maximum quiescent supply current of  $45\mu\text{A}$ , and (at  $400\mu\text{A}$  load current) a dropout of only 100mV. These devices provide  $0.12\mu\text{V}/\mu\text{A}$  load regulation and  $8\mu\text{V}/\text{V}$  line regulation, and they remain stable with load capacitance in the 0 to 2.2nF range. Prices start at \$0.45 (1000 up, FOB USA).

space-critical applications. They also provide stable operation for load capacitance up to 2.2nF. Low dropout voltage (200mV) and a very low supply current make these references ideal for low-voltage, battery-operated systems. Line and load regulation are  $<75\mu\text{V}/\text{V}$  and  $<0.2\mu\text{V}/\mu\text{A}$ , respectively.

The MAX6012/MAX6021/MAX6025/MAX6041/MAX6045/MAX6050 come in 3-pin SOT23 packages, with prices starting at \$1.35 (1000 up, FOB USA).



# NEW PRODUCTS

## 8:1 and dual 4:1 cal-muxes include precision resistor-dividers

The 8-channel MAX4539 and dual 4-channel MAX4540 are calibration multiplexers (cal-muxes) for self-monitoring applications and precision ADCs. Each device includes precision resistor-dividers for generating accurate references of  $V+/2$ ,  $5/8(V+ - V-)$ ,  $15V_{REF}/4096$ , and  $4081V_{REF}/4096$  (where  $V_{REF}$  is an external reference voltage).

The MAX4539/MAX4540 multiplexers have enable inputs and address latching. When operating with +5V or ±5V supplies, all digital inputs exhibit 0.8V/2.4V logic thresholds that ensure

TTL and CMOS compatibility. All inputs have protection diodes that ensure ESD ratings higher than 2kV.

Both devices operate from a single supply in the +2.7V to +12V range, or from dual supplies in the ±2.7V to ±6V range. On-resistances (100Ω max) are matched to within 12Ω max within a device, and each switch can handle Rail-to-Rail® analog signals. The off-leakage current is 1nA at  $T_A = +25^\circ\text{C}$  and 10nA at  $T_A = +85^\circ\text{C}$ .

The MAX4539/MAX4540 multiplexers are available in 20-pin SSOP, SO, and DIP packages. Prices start at \$2.84 (1000 up, FOB USA).

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

## 8th-order, lowpass, elliptic, switched-capacitor filters are clock-tunable

The MAX7400/MAX7403 8th-order elliptic, lowpass, switched-capacitor filters provide corner frequencies from 1Hz to 10kHz and draw supply currents of only 2mA. Operating from a single +5V power supply, they are well suited for low-power anti-aliasing and post-DAC filtering applications. Each has a shutdown mode that lowers the supply current to just 0.2μA.

The MAX7400 provides sharp rolloffs with a 1.5 transition ratio and 80dB of stopband rejection. The MAX7403 provides a sharper rolloff (1.2 transition ratio) with 58dB of stopband rejection. Both filters offer a low output offset (±4mV) that is adjustable via an offset-adjustment pin.

The filters' internal switching can be self-clocked with an external capacitor or clocked externally for tighter control of the corner frequency. Their fixed output response simplifies the design effort—just select a corner frequency by setting the clock frequency. MAX7400/MAX7403 filters are available in 8-pin SOIC and plastic DIP packages. Prices start at \$1.95 (1000 up, FOB USA).

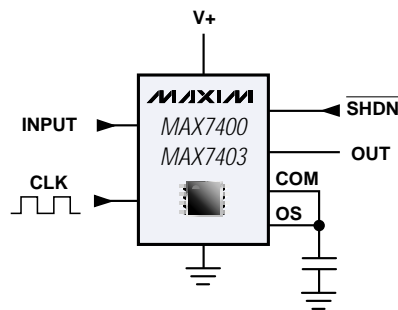
## 5th-order filters for \$0.99 save space and power

A new series of 5th-order, lowpass, switched-capacitor Bessel and Butterworth filters is available in 8-pin μMAX and DIP packages. The proprietary μMAX package, 80% smaller than an 8-pin DIP, makes them the smallest 5th-order switched-capacitor filters available in the industry. Operating on a single supply voltage of +5V (MAX7409/MAX7410) or +3V (MAX7413/MAX7414), they draw supply currents of only 1.2mA. Low cost, small size, and low-power operation make these filters highly suitable for cost-sensitive portable equipment requiring post-DAC filtering or anti-aliasing.

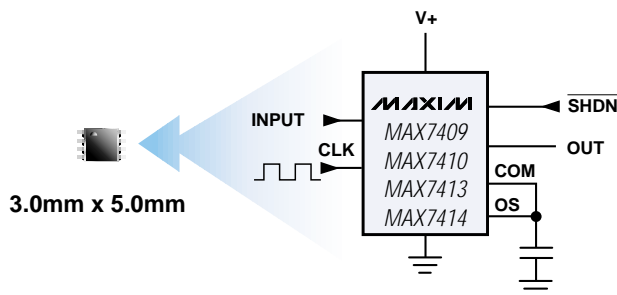
Bessel filters (MAX7409/MAX7413) provide low overshoot, fast settling, and linear phase response, and Butterworth filters (MAX7410/MAX7414) provide a maximally flat passband response. All four devices have a fixed response that reduces the design task to a simple selection of clock frequency.

Corner frequencies are clock tunable from 1Hz to 15kHz with a clock-to-corner ratio of 100. Two clocking options are available: self-clocking through the use of an external capacitor, or external clocking for tighter control of the cutoff frequency. Their low output offset (±4mV) can be adjusted through an offset-adjust pin.

The MAX7409/MAX7410/MAX7413/MAX7414 filters are available in 8-pin μMAX and plastic DIP packages, with prices starting at \$0.99 (100,000 up, FOB USA).



WORLD'S SMALLEST  
5TH-ORDER LOWPASS FILTER



# NEW PRODUCTS

## High-speed step-down controller for notebook CPUs has 4-bit digital control

The MAX1710 step-down controller, intended as a DC-DC converter for the core CPU in notebook computers, offers ultra-fast transient response, high DC accuracy, and the high efficiency needed in leading-edge CPU power supplies. Maxim's proprietary quick-response, constant-on-time control scheme (QUICK-PWM™) handles wide ratios of input/output voltage with ease, and maintains a relatively constant switching frequency while providing a 100ns "instant-on" response to load transients.

DC precision is ensured by a 2-wire remote-sensing scheme that compensates for voltage drops in the supply rail and the ground bus. An internal 4-bit DAC sets the output voltage in accordance with specifications of the Mobile Pentium II® CPU.

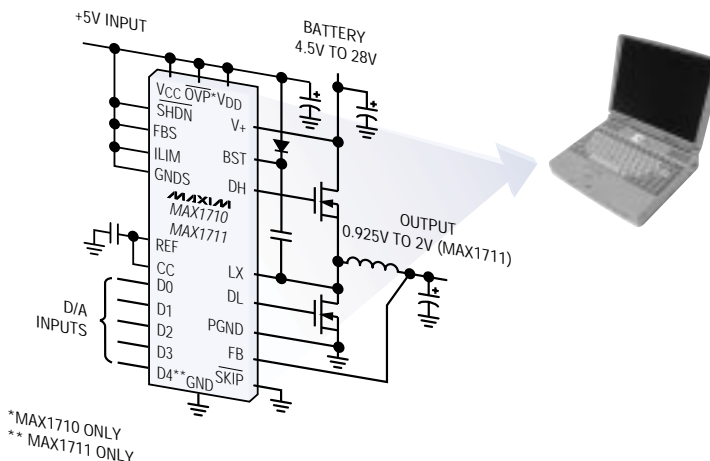
The MAX1710 achieves high efficiency at reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous-rectifier MOSFETs, made possible by powerful internal gate drivers with anti-shoot-through circuitry.

By stepping down high battery voltage directly, the MAX1710's single-stage buck conversion enables the highest possible efficiency. As an alternative, users can achieve the minimum physical size through two-stage conversion, by

employing a higher switching frequency and by stepping down the +5V system supply instead of the battery. The internal switching frequency is pin-programmable up to 550kHz, allowing the use of small, low-profile resistors and capacitors. The MAX1710 comes in a small 24-pin QSOP package with prices starting at \$3.89 (1000 up, FOB USA).

*QUICK-PWM is a trademark of Maxim Integrated Products.*

*Mobile Pentium II is a registered trademark of Intel Corp.*



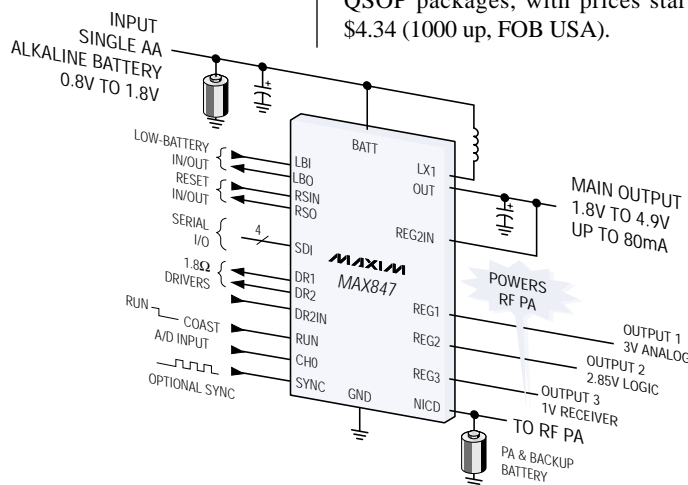
## ICs deliver complete power management for wireless transceivers

The MAX847 and MAX769 step-up DC-DC converters offer low-voltage operation, high efficiency, and synchronous rectification for 2-way pagers, GPS receivers, and other low-power digital wireless systems powered by 1-cell to 3-cell alkaline batteries. Offering guaranteed start-up for battery voltages as low as 0.87V, they operate with quiescent supply currents of 37µA each (2µA in shutdown).

An internal synchronous rectifier eliminates the need for an external Schottky diode. It also boosts the conversion efficiency to 90% and, for the MAX847, provides output currents higher than 50mA while operating from a single cell. The

MAX769, which provides step-up/step-down conversion while operating from two cells, delivers more than 90mA. An SPI-compatible serial interface enables the regulated output of each device to be digitally adjusted in 100mV increments between 1.8V and 4.9V. The no-load supply current is only 13µA.

Both chips include a multichannel ADC for battery monitoring and three low-noise linear-regulator outputs for various uses (3V analog, 2.85V logic, and 1V receiver). An evaluation kit for each device (MAX847EVKIT, MAX769EVKIT) is available to speed designs and aid in prototyping. Both devices are available in 28-pin QSOP packages, with prices starting at \$4.34 (1000 up, FOB USA).



# NEW PRODUCTS

## **PWM step-up DC-DC controllers deliver 20W power in tiny $\mu$ MAX packages**

The MAX668/MAX669 step-up DC-DC controllers feature fixed-frequency PWM control and deliver high power (to 20W) with efficiencies as high as 90%. Only 1.1mm high, they occupy half the area of an 8-pin SO package. Operating in step-up, SEPIC, flyback, or isolated-output configurations, the MAX668/MAX669 controllers extend battery life in cell phones, telecom hardware, POS systems, and wireless LANs. Their wide input-voltage range (1.8V to 28V) is well suited to systems powered by batteries and AC adapters.

By enabling PWM operation for moderate/heavy loads and pulsing only as needed for light loads, Maxim's proprietary Idle Mode™ control minimizes noise and optimizes efficiency. Users can set the constant PWM frequency as high as 500kHz to allow use of the smallest external components. A logic-controlled shutdown lowers the 220 $\mu$ A quiescent current to only 3.5 $\mu$ A.

The MAX669 runs in bootstrapped mode (powered by its own output voltage), accepts input voltages as low as 1.8V, and provides outputs as high as 28V. The MAX668 runs in either bootstrapped or normal mode. It accepts input voltages down to 3V, and (in normal mode) can boost the output voltage to levels limited only by the maximum operating voltage of the external N-channel switching MOSFET.

A preassembled evaluation kit (MAX668EVKIT) including recommended external components is available as an aid to minimize design time. MAX668/MAX669 controllers come in 10-pin  $\mu$ MAX packages, with prices starting at \$2.10 (1000 up, FOB USA).

*Idle Mode is a trademark of Maxim Integrated Products.*

## **Compact, high-efficiency DC-DC converters have low supply current**

The MAX1674/MAX1675/MAX1676 step-up DC-DC converters offer high efficiency (to 94%) in a tiny  $\mu$ MAX package. Quiescent supply currents are only 16 $\mu$ A, and their built-in synchronous rectifiers improve efficiency. By eliminating the need for an external Schottky rectifier, the synchronous rectifiers also reduce size and cost.

The MAX1674 has a 1A current limit; the MAX1675 has a lower 0.5A limit that permits use of a smaller inductor. The MAX1676 features an adjustable current

limit and internal circuitry that minimizes EMI by reducing the inductor-voltage ringing. All include a 0.3 $\Omega$ , N-channel MOSFET power switch, and all have pre-set, pin-selectable outputs of 3.3V or 5V. Outputs can also be set to any level between 2V and 5.5V using two external resistors. In each case, the input-voltage range is 0.7V to  $V_{OUT}$  and start-up is guaranteed for inputs down to 1.1V.

Other features include 94% efficiency at 200mA output current, an internal low-battery detector, and 0.1 $\mu$ A shutdown capability. A preassembled evaluation kit (MAX1676EVKIT) is available to speed the design process. These devices are available in 8-pin or 10-pin  $\mu$ MAX packages, with prices starting at \$1.85 (1000 up, FOB USA).

## **RS-232 transceiver offers low cost and small size**

The MAX254B\* is a complete, electrically isolated RS-232 interface for space- and cost-constrained applications. Intended for applications in which noise, high transient voltage, and differential ground potentials can damage equipment and corrupt communications, it integrates optocouplers with a transceiver and transformer in a small surface-mount package. As a single RS-232 transceiver containing one transmitter and one receiver, it is ideal for applications that do not require handshaking signals. (For those that do, please see the MAX252 data sheet.)

The MAX254B meets all EIA/TIA-232E and ITU V.28 specifications at data rates up to 100kbps. A single +5V supply on the logic side powers both the isolated and nonisolated sides of the interface. The isolated V+ and V- supplies can deliver 10mA of auxiliary power, and a shutdown-logic input allows the MAX254B to enter a 0.4 $\mu$ A low-power shutdown mode.

The MAX254B is available in a 24-pin wide SO package.

*\*The MAX254B is a future product—contact factory for availability.*

## **3.3V, 622Mbps, SDH/SONET 8:1 serializer includes clock synthesis and TTL inputs**

The MAX3690 serializer operates from a 3.3V supply, consumes 200mW, and converts 8-bit-wide, 77MHz parallel data to 622Mbps serial data in SDH/SONET systems. Other applications include add/drop multiplexers and digital cross connects.

The MAX3690 accepts TTL clock and data inputs, and delivers a 3.3V PECL serial-data output. A fully integrated phase-locked loop (PLL) synthesizes an internal 622Mbps serial clock from a low-speed crystal reference clock of 155.52MHz, 77.76MHz, 38.88MHz, or 51.84MHz. A TTL loss-of-lock output indicates whether the PLL is operating correctly.

The MAX3690 is available in a 32-pin TQFP package.

# NEW PRODUCTS

## Low-power, 2.5Gbps clock-recovery and data-retiming IC operates on +3.3V

The MAX3875 is a compact, low-power clock-recovery and data-retiming IC for 2.488Gbps SDH/SONET applications. Its fully integrated phase-locked loop recovers a synchronous clock signal from the serial NRZ data input, which is then retimed by the recovered clock. Differential PECL-compatible outputs are provided for both clock and data signals,

and the chip provides an additional 2.488Gbps serial input for system-loopback diagnostic testing. It also provides a TTL-compatible loss-of-lock monitor ( $\overline{\text{LOL}}$ ).

The MAX3875 is designed for both section-regenerator and terminal-receiver applications in OC-48/STM-16 transmission systems. Its jitter performance exceeds all SONET/SDH specifications. It operates from a single supply voltage of +3.3V to +5V. At +3.3V, it consumes only 400mW over the extended industrial temperature range (-40°C to +85°C). The MAX3875 is available in a 32-pin TQFP package.

## +3.3V, 2.5Gbps, SDH/SONET laser driver has automatic power control

The MAX3867 laser driver operates on +3.3V or +5V and draws less than 65mA of supply current at +3.3V. It accepts differential-PECL data and clock inputs to 2.5Gbps, and provides bias and modulation currents for the laser. The synchronizing input latch can be bypassed if a clock signal is not available.

Automatic power control (APC) feedback maintains a constant average optical power over temperature and lifetime. The wide ranges of modulation current (5mA to 60mA) and bias current (1mA to 100mA) are easy to program, making the MAX3867 an excellent choice for various SDH/SONET applications. It complies with ANSI, ITU, and Bellcore SONET/SDH specifications.

The MAX3867 also provides an enable control, a programmable slow-start circuit for setting the laser turn-on delay, and a failure-monitor output that indicates when the APC loop is unable to maintain the average optical power. It is available in a small 48-pin TQFP package.

## Low-cost direct-conversion tuner IC is designed for digital DBS applications

The MAX2105 direct-conversion tuner IC is designed for use in set-top boxes for DBS (digital direct-broadcast satellite) television. Its direct-conversion architecture (vs. an IF-based architecture) offers the lowest cost available. Operating from a single +5V supply, it accepts input frequencies from 950MHz to 2150MHz and employs a broadband I/Q downconverter to directly tune L-band signals to baseband.

The MAX2105 includes a low-noise amplifier (LNA) with automatic gain control (AGC), two downconverter mixers, an oscillator buffer with 90° quadrature generator and prescaler, and baseband amplifiers. Its reduced AGC range (41dB) allows input power levels down to -60dBm. This reduced-range AGC allows the MAX2105 to achieve a lower system noise figure through use of a high-gain external LNA. It also provides automatic baseband-offset correction.

An evaluation kit is available to speed the design cycle. The MAX2105 is available in a 28-pin SO package, with prices starting at \$4.50 (1000 up, FOB USA), and dropping to the \$2 range in high volumes.

## Upconverter mixers operate from 400MHz to 2.5GHz

The MAX2660/MAX2661/MAX2663 and MAX2671/MAX2673 high-linearity upconverter mixers are low-cost, low-noise, miniature devices with the best linearity vs. supply current trade-off of any bipolar mixer available. They are ideal for low-voltage operation in portable consumer equipment. Their double-balanced mixers combine IF frequencies in the 40MHz to 500MHz range with local-oscillator signals, upconverting them to output frequencies as high as 2.5GHz. Applications include 400MHz/900MHz/2.5GHz ISM, hand-held radios, cellular and cordless telephones, wireless LANs, and PCS systems.

A wide range of supply currents and output-intercept levels enable these devices to optimize performance in a system. Their supply current is essentially constant over the specified range of supply voltage. The MAX2663 requires only 3mA of supply current and provides an OIP3 of 0.7dB. The MAX2671 requires an 11.8mA supply current and provides an OIP3 of 9.6dB. For the typical configuration of  $V_{\text{SHDN}} = 0$ , a shutdown mode lowers the supply current to less than 1 $\mu$ A.

For applications that require balanced IF ports, choose the MAX2673 in an 8-pin  $\mu$ MAX package. The MAX2660/MAX2661/MAX2663/MAX2671 are available in space-saving 6-pin SOT23 packages. Prices start at \$0.76 (1000 up, FOB USA).

